

FIG. 1

FIG. 1 is a block diagram of a processor architecture.

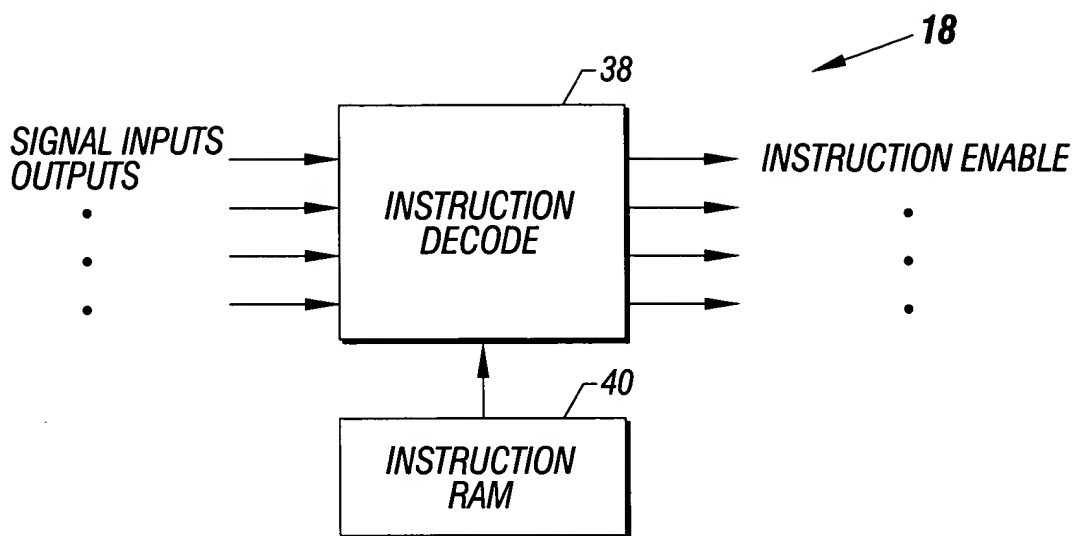


FIG. 2

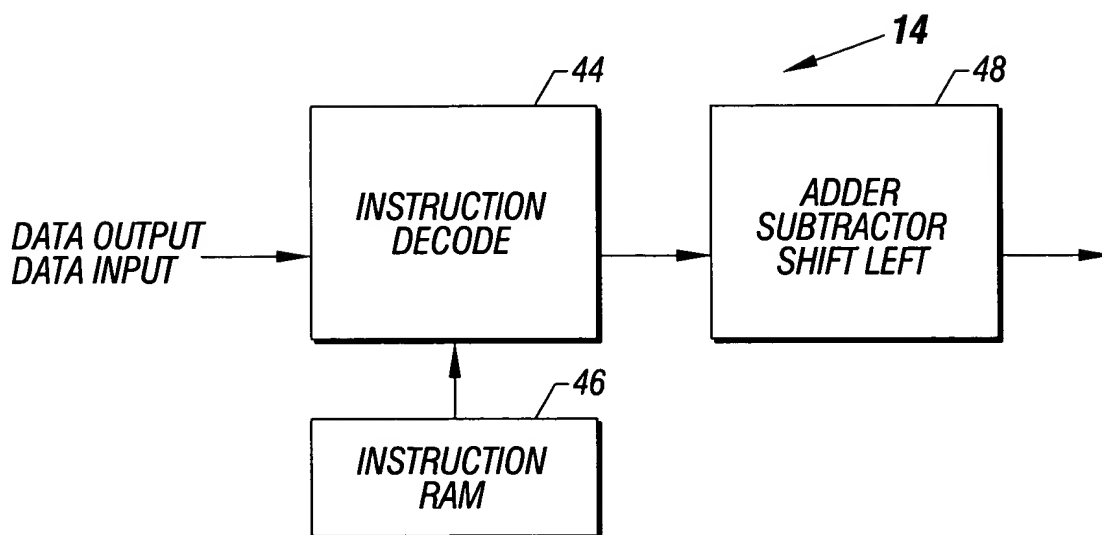
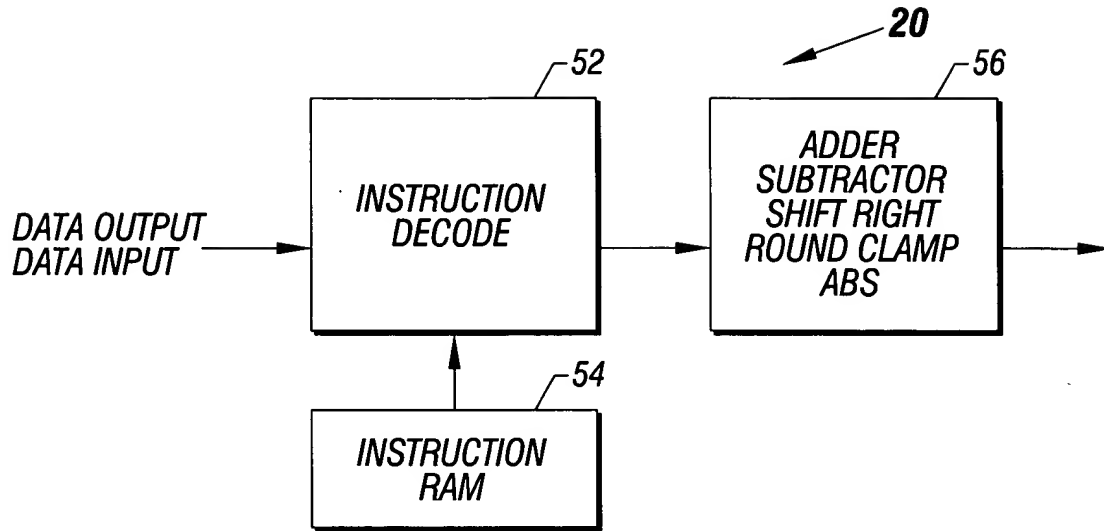
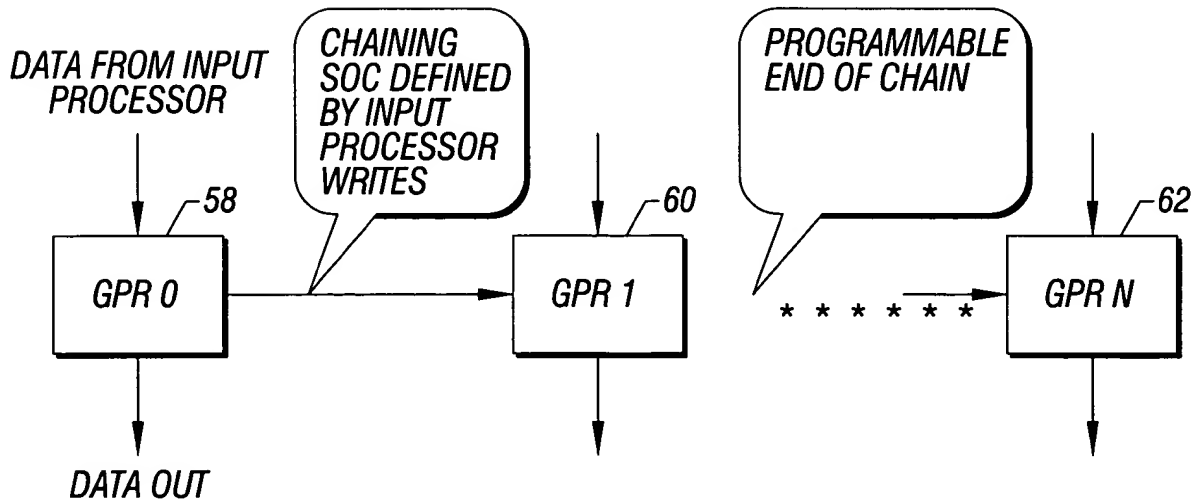


FIG. 3



**FIG. 4**



**FIG. 5**

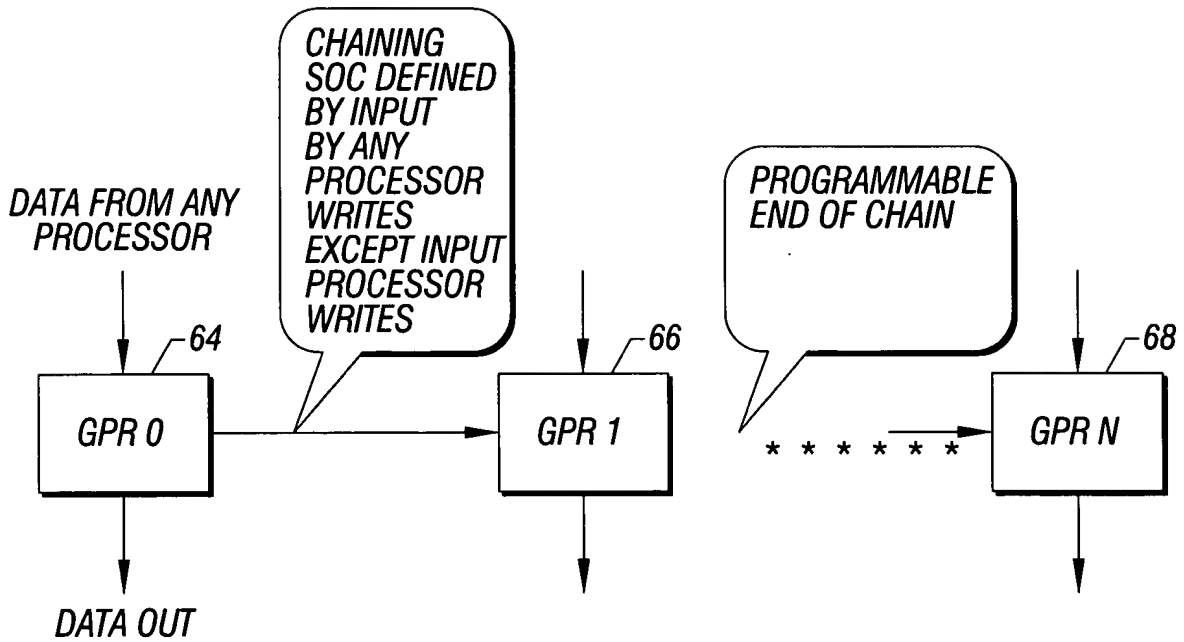


FIG. 6

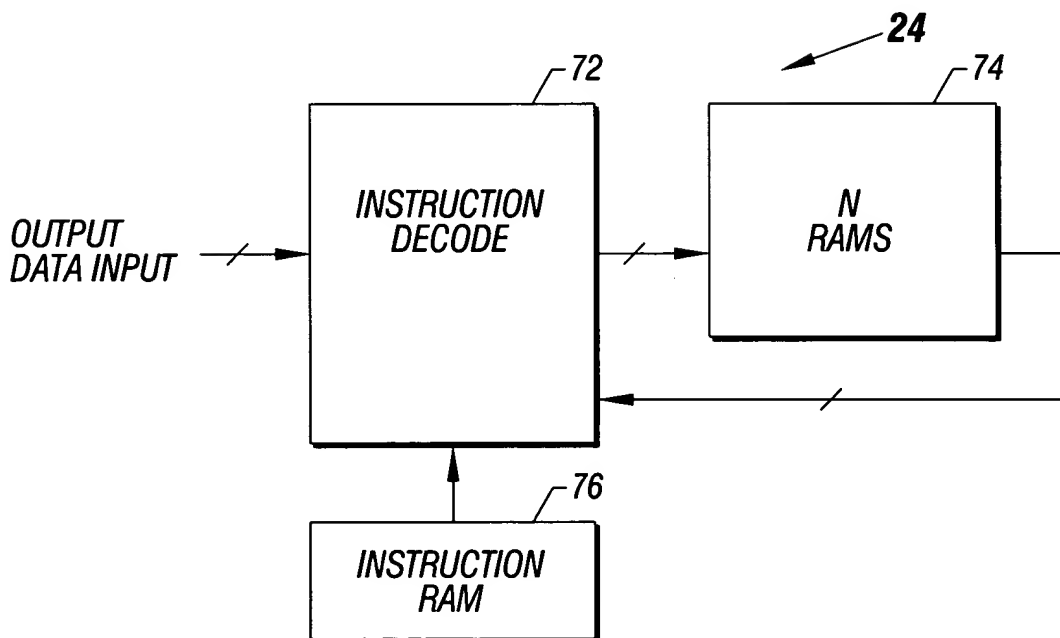
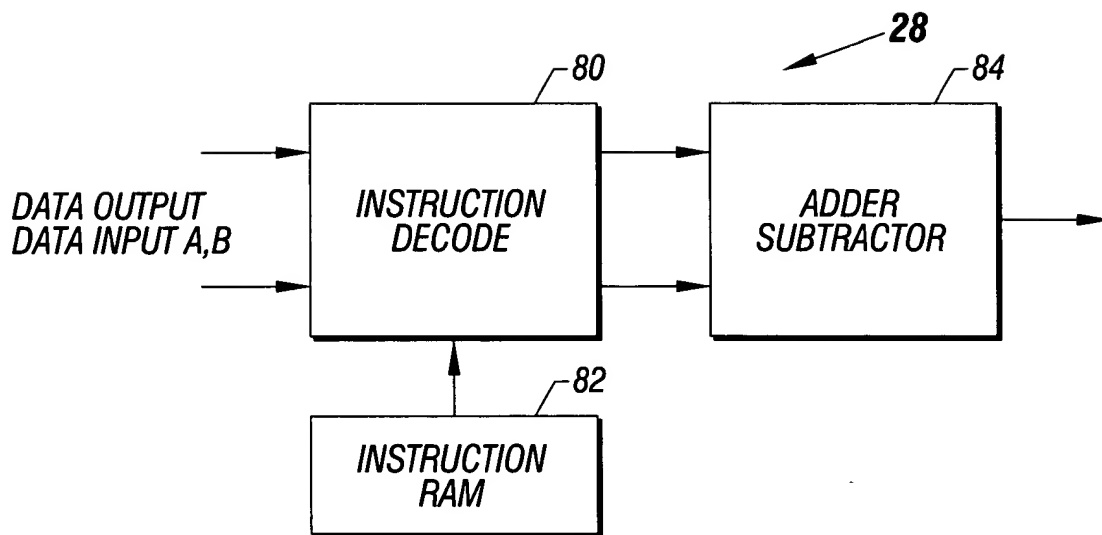
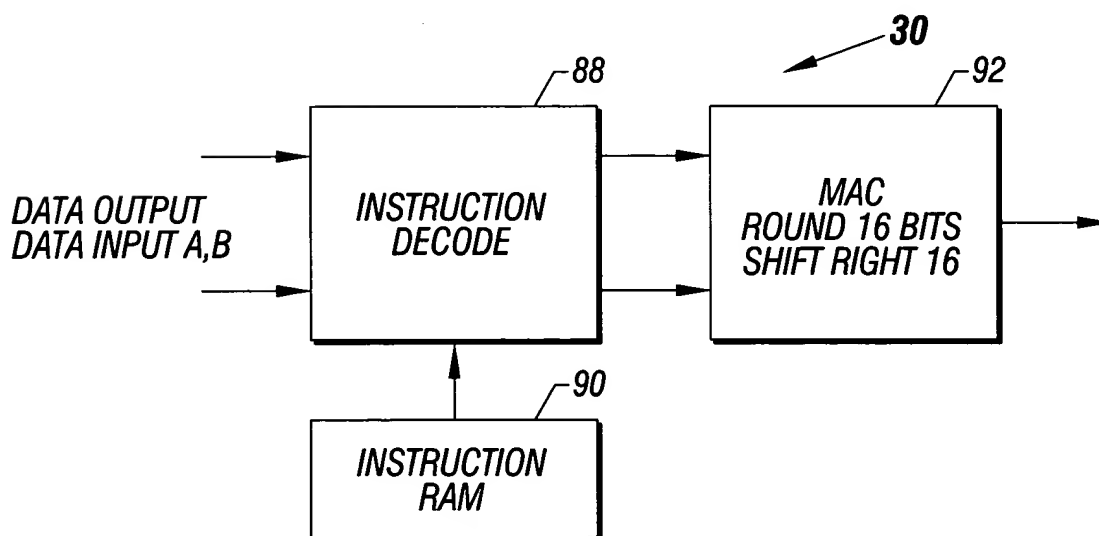


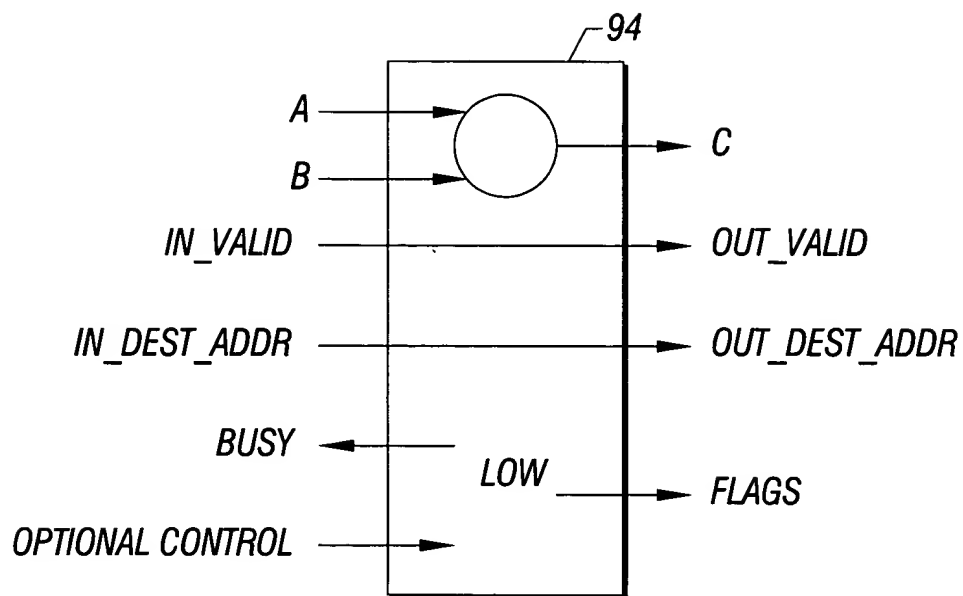
FIG. 7



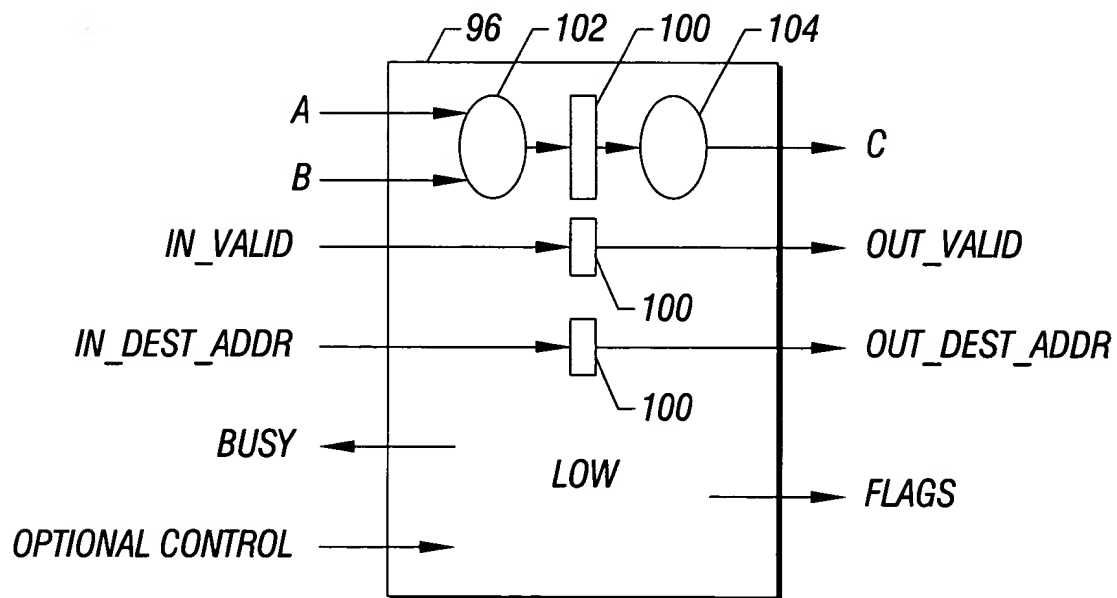
**FIG. 8**



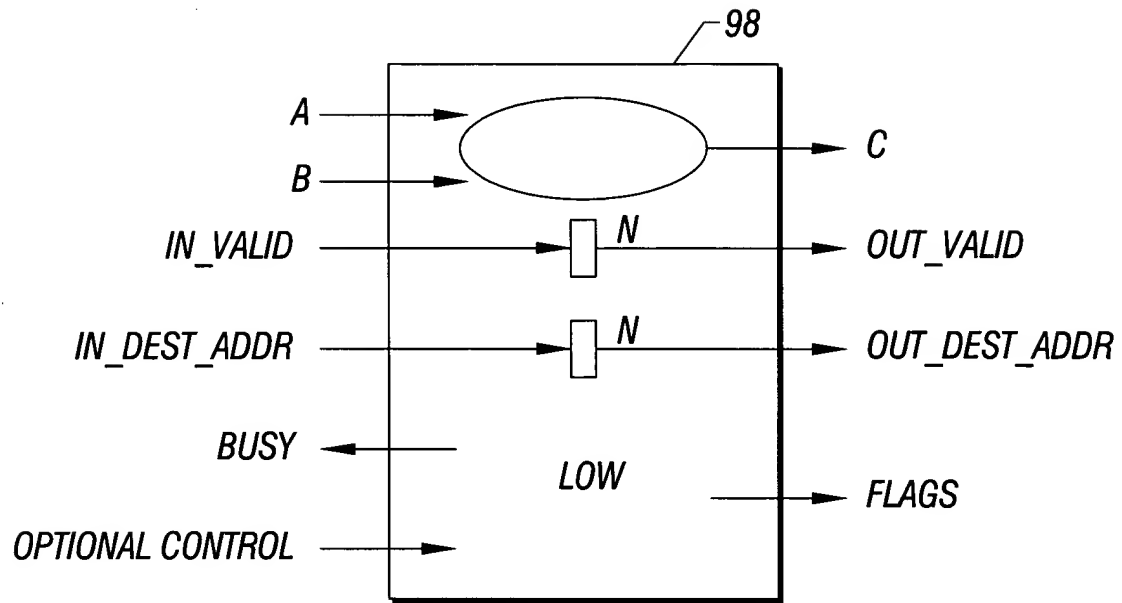
**FIG. 9**



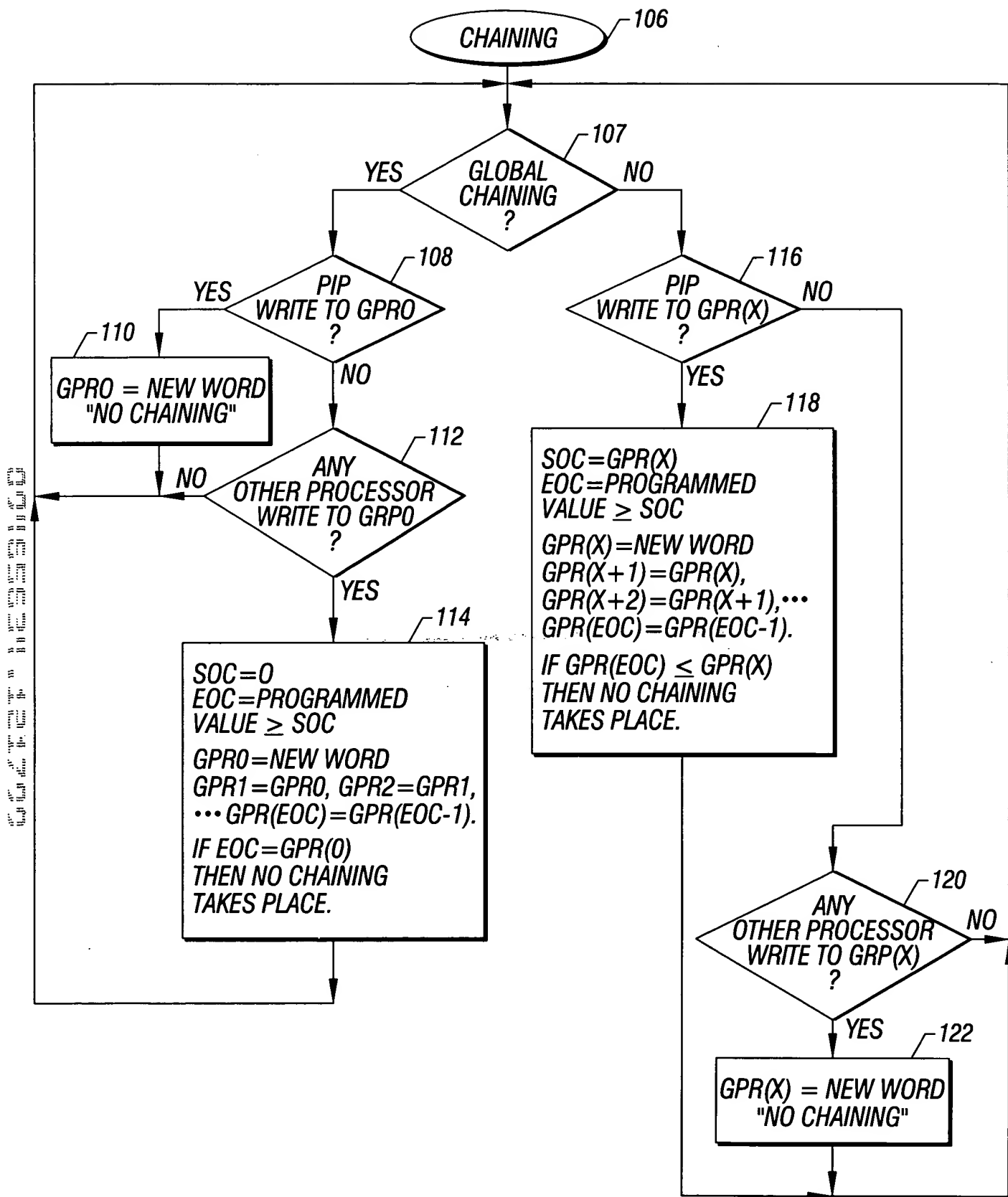
**FIG. 10**



**FIG. 11**



**FIG. 12**



**FIG. 13**